REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 61, 62, 73-76, and 79-87 stand rejected under 35 USC 103(a) as allegedly being unpatentable over the admitted prior art in view of Tang. The claims have been amended to better emphasize the patentable distinctions, and it is respectfully suggested that as amended, the claims are not rendered obvious by this hypothetical combination.

One aspect of the present invention is the recognition of a specialized problem in a thin film transistor on an insulating surface. Generally, such a semiconductor film is quite thin, in order to maintain positive characteristics of the thin film. However, when the film is very thin, e.g. as thin as hundreds of Angstroms, it may be difficult to form contacts on the semiconductor. Fabrication of the contact holes may cause overetching. This may also cause holes or pits in the thin film. See page 1 of the specification, second and third full paragraphs. The admitted prior art does not in any way teach or suggest this problem, nor does Tang.

The present claims define a solution. In order to prevent defects at the contacts, a layer that has metal is provided on the insulating substrate and is in direct contact with an

interconnection, and is connected with one of the source and drain regions. One of the reasons why this limitation is patentable, however, is that this not only recognizes a solution, but also recognizes a problem: defects at the contacts of the semiconductor thin film on the insulating substrate.

In view of the above amendments and remarks, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be allowed. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Version with markings to show changes made

In the claims:

Claims 61, 73-76, 81, 83, and 85-87 have been amended as follows:

61. (Amended) A display device comprising:

[a substrate;]

a semiconductor island comprising silicon provided [over said substrate] on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[a gate] an interconnection [provided in a same layer as said gate electrode] formed on said insulating surface;

a layer comprising metal provided [over said substrate] on said insulating surface and being in direct contact with said [gate] interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole.

73. (Amended) A semiconductor device comprising:

[a substrate;]

a semiconductor island comprising silicon provided [over said substrate] on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[a gate] an interconnection [provided in a same layer as said gate electrode] formed on said insulating surface;

a layer comprising metal provided [over said substrate] on said insulating surface and being in direct contact with said [gate] interconnection and being connected with one of said source region and said drain region, said layer comprising metal

being connected with said [gate] interconnection through no contact hole;

an interlayer dielectric provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole.

74. (Amended) A semiconductor device comprising:

[a substrate;]

a semiconductor island comprising silicon provided [over said substrate] on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[a gate] an interconnection [provided in a same layer as said gate electrode] formed on said insulating surface;

a layer comprising metal provided [over said substrate] on said insulating surface and being in direct contact with said [gate] interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric comprising silicon nitride provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole.

75. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said [substrate] insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[a gate] an interconnection [provided in a same layer as said gate electrode] formed on said insulating surface;

a layer comprising metal provided [over said substrate] on said insulating surface and being in direct contact with said [gate] interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric comprising silicon oxide provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole.

76. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said [substrate] insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode comprising a doped polycrystalline silicon provided adjacent to said channel region with a gate insulating film therebetween;

[a gate] an interconnection [provided in a same layer as said gate electrode] formed on said insulating surface;

a layer comprising metal provided [over said substrate] on said insulating surface and being in direct contact with said [gate] interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole.

81. (Amended) The device of claim 74 wherein said [metal] layer comprising metal is connected with said [gate interconnect] interconnection through no contact hole.

83. (Amended) The device of claim 75 wherein said [metal] layer comprising metal is connected with said [gate interconnect] interconnection through no contact hole.

85. (Amended) The device of claim 76 wherein said [metal] layer comprising metal is connected with said [gate interconnect] interconnection through no contact hole.

86. (Amended) A display device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said [substrate] insulating surface;

a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[a gate] an interconnection [provided in a same layer as said gate electrode] formed on said insulating surface;

a layer comprising said metal provided [over said substrate] on said insulating surface and being in direct

contact with said [gate] interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said layer comprising said metal;

a contact hole provided over said layer comprising said metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising said metal through said contact hole.

87. (Amended) A semiconductor device comprising:

[a substrate;]

a semiconductor island comprising silicon provided [over said substrate] on an insulating surface;

a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

[a gate] an interconnection [provided in a same layer as said gate electrode] formed on said insulating surface;

a layer comprising said metal provided [over said substrate] on said insulating surface and being in direct contact with said [gate] interconnection and being connected with one of said source region and said drain region, said layer comprising said metal being connected with said [gate] interconnection through no contact hole;

an interlayer dielectric provided over said gate electrode and said layer comprising said metal;

a contact hole provided over said layer comprising said metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising said metal through said contact hole.